CLAIMS

What is claimed is:

1. An anti-wafer structure for testing a plurality of dice on a wafer under test, the structure comprising:

a silicon on insulator (SOI) layer; and

a plurality of probe dice formed on the SOI layer, each probe die in the plurality of probe dice having a pad layout corresponding to a pad layout of a die on the wafer under test.

2. The anti-wafer structure of claim 1 further comprising:

a plurality of holes extending through the SOI layer and the plurality of probe dice, the holes corresponding to pads on the probe dice.

3. The anti-wafer structure of claim 2 wherein the holes are filed with interconnect lines coupled to form electrical connections on either side of the anti-wafer structure.

4. The anti-wafer structure of claim 3 wherein the interconnect lines are coupled to pads of the wafer under test.

5. The anti-wafer structure of claim 1 wherein a number of the probe dice equals a number of dice on the wafer under test.

6. The anti-wafer structure of claim 1 wherein the SOI layer comprises an oxide layer.

7. The anti-wafer structure of claim 1 further comprising an adapter layer configured to adapt a pad layout of a probe die to another pad layout.

8. A probe card for testing dice on a wafer under test, the probe card comprising:

a board for interfacing to a tester;

an anti-wafer having a plurality of probe dice, the anti-wafer having a plurality of interconnect lines extending through holes in the anti-wafer, the plurality of interconnect lines coupling pads of the anti-wafer to the board; and

an elastomer located between the anti-wafer and the wafer under test, the elastomer providing an electrical connection between pads of the wafer under test and the pads of the anti-wafer.

9. The probe card of claim 8 further comprising a ceramic disk, and wherein the holes extend through the ceramic disk and the board.

10. The probe card of claim 8 wherein the probe dice are mirror-images of dice on the wafer under test.

11. The probe card of claim 8 wherein the board comprises a printed circuit board.

12. A method of fabricating an anti-wafer, comprising:

providing a substrate, an SOI layer over the substrate, and a silicon layer over the SOI layer;

forming a seal layer over the silicon layer;

removing the substrate;

forming an opening through the SOI layer and the silicon layer; and

removing the seal layer.

13. The method of claim 12 further comprising:

forming an interconnect line extending through the SOI layer and the silicon layer.

14. The method of claim 13 wherein the substrate is removed using a polishing process.

15. The method of claim 14 further comprising:

performing an HF dip process to clean a surface of the SOI layer after the polishing process.

16. The method of claim 15 further comprising:

depositing an oxide on the SOI layer after the HF dip process.

17. The method of claim 12 wherein the seal layer comprises:

an oxide layer over the silicon layer; and

a nitride layer over the oxide layer.

18. The method of claim 12 wherein the silicon layer includes pad openings and the seal layer protects the pad openings during subsequent processing steps.

19. The method of claim 12 wherein the SOI layer comprises silicon dioxide.

20. The method of claim 12 wherein the substrate comprises a silicon substrate.